REMARKS

This Amendment is in response to the Office Action dated May 19, 2004. Claims 9-22 are pending in the present application. Claims 9-22 have been rejected. Claims 1-8 have been withdrawn from consideration. Claims 9, 13, 18-20 have been amended to overcome Examiner's objections. Claims 10-12 and 14-16 have been cancelled. Consequently, claims 9, 13 and 17-22 remain pending in the present application.

The Examiner has stated:

1. The abstract of the disclosure is objected to because it contains legal language such as comprises. Correction is required. See MPEP § 608.01(b).

The abstract has been corrected in accordance with the Examiner's instructions.

Claim Rejections – 35 U.S.C. 103

The Examiner has stated,

2. The following is a quotation of 35 U.S. C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 9-12 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ellul et al. in view of Thomas et al.

Regarding claim 9, Ellul et al. (US 5,614,750) teaches a semiconductor device [Figure 6] comprising a substrate 52, a plurality of device structures 90, a buried layer 54, an interconnect comprising a slot 78, a conductive material 82 in the slot, oxidized sidewalls 80 which forms a sinker to the buried layer [column 4, lines 63-67]. Thomas et al. (US 4,933,743) teaches a metal 26 in a slot to form an interconnect. It would have been obvious to one of ordinary skill in the art to use a

metal in the device of Ellul et al. since Ellul et al. teaches the use of other conductive materials such as those taught by Thomas et al.

Regarding claims 10-12, Thomas et al. further teaches multiple metals in the interconnect slot which partially fill the slot with a final metal which provides the interconnect layer. It would have been obvious to one of ordinary skill in the art to use the multiple metals of Thomas et al. in the device Ellul et al. since the structure of Thomas et al. provides lower resistance and improved electromigration resistance [column 2, lines 63-67].

Regarding claim 17, Ellul et al. further teaches a sinker coupled to a collector 55.

4. Claims 13 - 16 and 18 - 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ellul et al. in view of Thomas et al.

Regarding claim 13, Ellul et al. teaches a semiconductor device [Figure 6] comprising a buried layer 54, an interconnect comprising a slot 78, a conductive material 82 in the slot, oxidized sidewalls 80 which forms a sinker to the buried layer [column 4, lines 63-67]. Thomas et al. teaches a metal 26 in a slot to form an interconnect. It would have been obvious to one of ordinary skill in the art to use a metal in the device of Ellul et al. since Ellul et al. teaches the use of other conductive materials such as those taught by Thomas et al.

Regarding claims 14 - 16, 20, and 22, Thomas et al. further teaches multiple metals in the interconnect slot which partially fill the slot with a final metal which provides the interconnect layer where the high current carrying conductors are on the same level [Figure 1L]. It would have been obvious to one of ordinary skill in the art to use the multiple metals of Thomas et al. in the device Ellul et al. since the structure of Thomas et al. provides lower resistance and improved electromigration resistance [column 2, lines 63-67].

Regarding claim 18, Ellul et al. further teaches a slot coupled to the emitter 94.

Regarding claims 19 and 21, Ellul et al. further teaches a CMOS integrated circuit structure with a bipolar device. Thomas et al. teaches an integrated circuit with bipolar and MOS logic circuits on the same device [column 1, lines 12-25]. It would have been obvious to one of ordinary skill in the art to use the device of EUul et al. in an 1C comprising bipolar transistors and MOS transistors since these are well known in the art as devices integrated on the same circuit using high voltage interconnects.

The Examiner has further stated:

Response to Arguments

5. Applicant's arguments filed October 14, 2003 have been fully considered but they are not persuasive.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); In re

Merck & Co., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Applicant argues that neither Ellul et al. nor Thomas et al. teach the limitations of the claimed invention, but no arguments are made against the combination of Ellul et al. and Thomas et al. as used in the preceding rejection.

Arguments should be directed to the combination of Ellul et al. and Thomas et al. and the motivation to combine them.

Further, applicant alleges that Thomas only teaches the use of an interconnect system on top of the substrate. Thomas et al. teaches a metal 26 in a slot to form an interconnect. This teaching is used in combination with Ellul et al. to meet the limitations of claims 9 - 22 as described above.

Applicant respectfully traverses this rejection.

Ellul describes in the Abstract:

"A buried layer contact for a integrated circuit structure is provided, with particular application for a contact for a buried collector of a bipolar transistor. The buried layer contact takes the form of a sinker comprising a fully recessed trench isolated structure having dielectric lined sidewalls and filled with conductive material, e.g. doped polysilicon which contacts the buried layer. The trench isolated contact is more compact than a conventional diffused sinker structure, and thus beneficially allows for reduced transistor area. Advantageously, a reduced area sinker reduces the parasitic capacitance and power dissipation. In a practical implementation, the structure provides for an annular collector contact structure to reduce collector resistance."

Referring to column 4, lines 58-61 of Ellul," The trench is lined with dielectric spacers 80, and filled with a conductive layer 82. "The conductive layer 82 comprising heavily doped polysilicon" (emphasis added). Providing polysilicon with a slot is clearly different from providing a metal within the slot. The metal within the slot allows for high power, high current operation of semiconductor device.

Thomas describes an interconnect system which includes metal layers to form different layers of metal contacts. The combination of Ellul and Thomas would describe a contact for a buried collector of a bipolar transistor coupled to an interconnect system. This combination is clearly different from the recited invention.

A key element of the present invention is that the interconnect includes "a plurality of metals within the slot wherein the plurality of metals comprises three metals, wherein the first and second metals fill the slot and the third metal provides an interconnect layer" as recited in claims 9 and 13. Neither Ellul or Thomas singly or in combination describes or suggests the plurality of metals or their cooperation with the other elements of the claims.

Accordingly, claims 9 and 13 are allowable over the cited references. In addition, claims 13 and 17-22 are allowable because they depend from allowable base claims.

Accordingly, Applicant respectfully submits that claims 9, 13 and 17-22 are now all in allowable form. Consequently, allowance and passage to issue of claims 9, 13 and 17-22 of the present application are respectfully requested.

Accordingly, Applicant's attorney believes that this application is in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,
SAWYER LAW GROUP LLP

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Date

Joseph A. Sawyer, Jr.
Attorney for Applicant
Reg. No. 30,801
(650) 493-4540